ABSTRACT OF THE DISCLOSURE

In a differential output signal circuit suitable for restraining voltage overshooting/undershooting at differential output terminals due to lags in input signals and realizing stable and fast switching of differential input signals, a first differential pair of PMOS transistors connected to a first current source and a second differential pair of NMOS transistors connected to a second current source are mutually connected at the differential output terminals, and a capacitor is connected between the connection nodes of the respective differential pairs and current sources. A transitional current path of the capacitor restrains voltage variations during differential input signal switching. Further in a signal detection apparatus suitable for realizing the detection of fast transmitted differential input signals with less current consumption and at low cost, an edge detect signal is supplied against a differential input of or above a prescribed value, and a setting signal is issued when this edge detect signal has been detected a prescribed number of times during a first prescribed length of time while a resetting signal is issued if none is detected during a second prescribed length of time. A signal-detect signal is generated from these setting signal and resetting signal.